

Claims

[c1] What is claimed is:

1. A damascene process capable of avoiding via resist poisoning, the damascene process comprising:
providing a semiconductor substrate with a low-k dielectric layer($k \leq 2.9$)thereon, a SiC layer over the low-k dielectric layer, a metal layer over the SiC layer, and a first bottom anti-reflection coating(BARC) layer over the metal layer;
forming a first resist layer on the first BARC layer,
wherein the first resist layer has a trench opening to expose a portion of the first BARC layer;
etching through the first BARC layer and the metal layer and etching a portion of the SiC layer to form a trench structure in the SiC layer;
removing the first resist layer and the first BARC layer;
forming a blocking layer on the surface of the trench structure of the SiC layer, wherein the blocking layer is used to prevent unpolymerized precursors diffused out from the low-k dielectric layer from contacting an overlying resist;
forming a second BARC layer on the blocking layer, the second BARC layer filling the trench structure;

forming a second resist layer on the second BARC layer, the second resist layer having a via opening to expose a portion of the second BARC layer;
etching through the second BARC layer, the SiC layer, and the blocking layer, and etching a portion of the low-k dielectric layer to form a via structure in the low-k dielectric layer;
removing the second resist layer and the second BARC layer; and
performing a dual damascene process using the metal layer and the SiC layer as masks to make the low-k dielectric layer form a dual damascene structure having the trench and the via structure.

- [c2] 2. The process of claim 1 wherein the blocking layer is formed by Ar plasma hitting the SiC layer.
- [c3] 3. The process of claim 2 wherein the Ar plasma comprises a fluorine substance.
- [c4] 4. The process of claim 3 wherein the fluorine substance is CF_4 .
- [c5] 5. The process of claim 1 wherein the low-k dielectric layer comprises a carbon-doped oxide (CDO) substance.
- [c6] 6. The process of claim 1 wherein a dielectric layer is set between the metal layer and the first BARC layer.

- [c7] 7. The process of claim 1 wherein the thickness of the SiC layer is less than 700 angstroms.
- [c8] 8. A damascene process capable of avoiding via resist poisoning, the damascene process comprising:
providing a semiconductor substrate with a low-k dielectric layer($k \leq 2.9$)thereon, and a SiC layer over the low-k dielectric layer;
forming a blocking layer on the SiC layer, wherein the blocking layer is used to prevent unpolymerized precursors diffused out from the low-k dielectric layer from contacting overlying resist;
forming a BARC layer on the blocking layer;
forming a resist layer on the BARC layer, wherein the resist layer has a via opening to expose a portion of the BARC layer; and
etching through the BARC layer, the blocking layer, and the SiC layer, and etching a portion of the low-k dielectric layer to form a single damascene structure in the low-k dielectric layer.
- [c9] 9. The process of claim 8 wherein the blocking layer is formed by Ar plasma hitting the SiC layer.
- [c10] 10. The process of claim 9 wherein the Ar plasma com-

prises a flurane substance.

- [c11] 11. The process of claim 10 wherein the flurane substance is CF_4 .
- [c12] 12. The process of claim 8 wherein the low-k dielectric layer comprises a carbon-doped oxide substance.
- [c13] 13. The process of claim 1 wherein the thickness of the SiC layer is less than 700 angstroms.